

DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Methods For Forming Wordlines, Transistor Gates, And Conductive Interconnects, And Wordline, Transistor Gate, and Conductive Interconnect Structures, Serial No. 09/332,271, filed June 11, 1999.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States

1 Code and that such willful false statement may jeopardize the validity of the
2 application or any patent issued therefrom.

3 * * * * *

4 Full name of inventor: Klaus Florian Schuegraf

5 Inventor's Signature: _____

6 Date: _____

7 Residence: Aliso Viejo, California

8 Citizenship: U.S.

9 Post Office Address: 26895 Aliso Creek Rd., Ste. D
10 Box 125
Aliso Viejo, CA 92656

1
2 Full name of inventor: Randhir P.S. Thakur

3 Inventor's Signature: _____

4 Date: _____

5 Residence: San Jose, California

6 Citizenship: India

7 Post Office Address: 5261 Apennines Circle, San Jose, CA 95138

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/332,271
 Filing Date June 11, 1999
 Inventor Klaus Florian Schuegraf et al.
 Assignee Micron Technology, Inc.
 Group Art Unit 2811
 Examiner Unknown
 Attorney's Docket No. MI22-532
 Title: Methods for Forming Wordlines, Transistor Gates, and Conductive
 Interconnects, and Wordline, Transistor Gate, and Conductive Interconnect
 Structures

FAX RECEIVED

SEP 29 2000

DECLARATION OF DAVID G. LATWESEN


PETITIONED OFFICE

1. I, David G. Latwesen, am a shareholder of the law firm of Wells, St. John, Roberts, Gregory & Matkin, P.S.

2. I hereby declare that I verified Mr. Schuegraf's last known address at 26895 Aliso Creek Rd., Suite D, Box 125, Aliso Viejo, CA 92656. I acquired the phone number of the address at 26895 Aliso Creek Rd., Suite D, Box 125, Aliso Viejo, CA 92656, through the online (telephonic online) directory service. I called the number and a female answered. I asked for Mr. Schuegraf. The female stated Mr. Schuegraf was at work. I then inquired as to whom I was speaking, and the female stated she was Mr. Schuegraf's wife. Mr. D. Brent Kenady, an associate of the firm, witnessed my end of this conversation.

3. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and, further, that these statements were made with knowledge that willful false statements and the like so made are punishable

1 by fine or imprisonment, or both, under §1001 of Title 18 of the United
2 States Code and that such willful false statements may jeopardize the validity
3 of the application or any patent issued thereon.
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24



DAVID G. LATWESEN
Reg. No. 38,533

1 **IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

2 Application Serial No. 09/332,271
 3 Filing Date June 11, 1999
 4 Inventor Klaus Florian Schuegraf et al.
 5 Assignee Micron Technology, Inc.
 6 Group Art Unit 2811
 7 Examiner Unknown
 8 Attorney's Docket No. MI22-532
 9 Title: Methods For Forming Wordlines, Transistor Gates, And Conductiv
 10 Interconnects, And Wordline, Transistor Gate, and Conductive Interconnect
 11 Structures

12 FAX RECEIVED

13 SEP 29 2000

14 **DECLARATION OF KAREN BRASEFIELD**

15 PATENT OFFICE

16 1. I, Karen Brasefield, am employed as a legal assistant at the law
 17 firm of Wells, St. John, Roberts, Gregory & Matkin, P.S.

18 2. One of the duties of my employment was to forward papers
 19 pertaining to the above-identified application to the inventor, Mr. Klaus
 20 Florian Schuegraf, for his signature.

21 3. I hereby declare that I prepared true copies of the above-entitled
 22 specification, claims and abstract, drawings, Declaration, and Assignment, as
 23 well as a certified mail label, return postcard receipt and the
 September 6, 2000 cover letter to Mr. Schuegraf, and presented same to our
 mail clerk for mailing, as is policy in this firm.

4. Our records indicate that true copies of the above-entitled
 specification, claims and abstract (21 pages), drawings (3 sheets), Declaration
 (3 pages), and Assignment (4 pages) were forwarded to Mr. Schuegraf by the
 United States Mail on September 6, 2000, to his address at 26895 Aliso Creek

1 Rd., Box 125, Ste. D, Aliso Viejo, CA 92656. However, the signature papers
2 w re never signed and returned.

3 5. True copies of the certified mail label, return postcard receipt
4 and the September 6, 2000 cover letter to Mr. Schuegraf are attached.

5 6. I hereby declare that all statements made herein of my own
6 knowledge are true and that all statements made on information and belief
7 are believed to be true and, further, that these statements were made with
8 knowledge that willful false statements and the like so made are punishable
9 by fine or imprisonment, or both, under §1001 of Title 18 of the United
10 States Code and that such willful false statements may jeopardize the validity
11 of the application or any patent issued thereon.

12
13 Dated: 9/21/00

Karen S. Brasefield
Karen S. Brasefield